

FIG. 1A
(PRIOR ART)

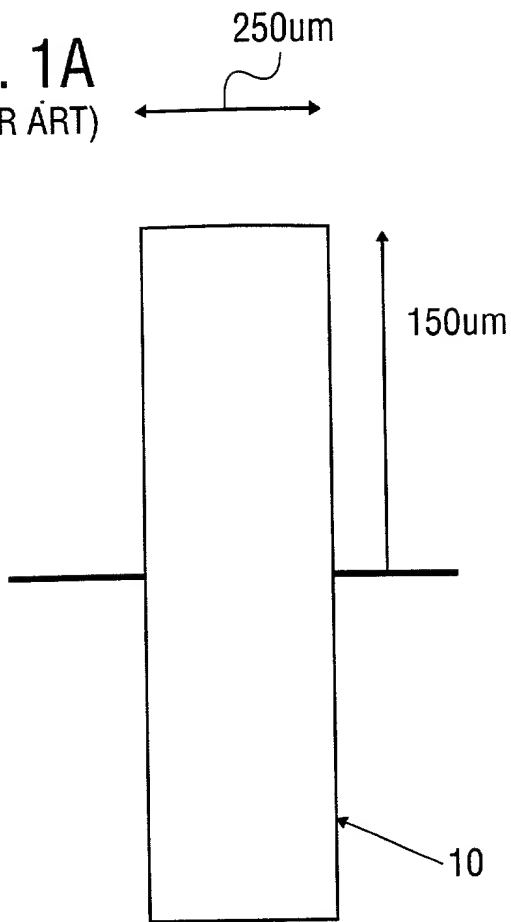


FIG. 1B
(PRIOR ART)

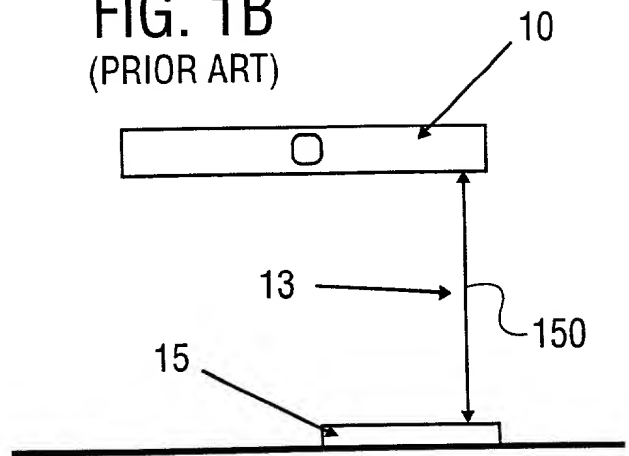
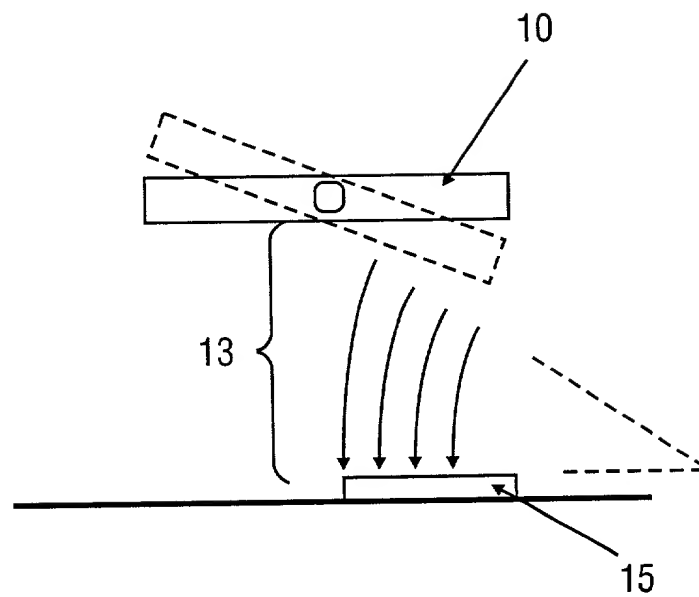
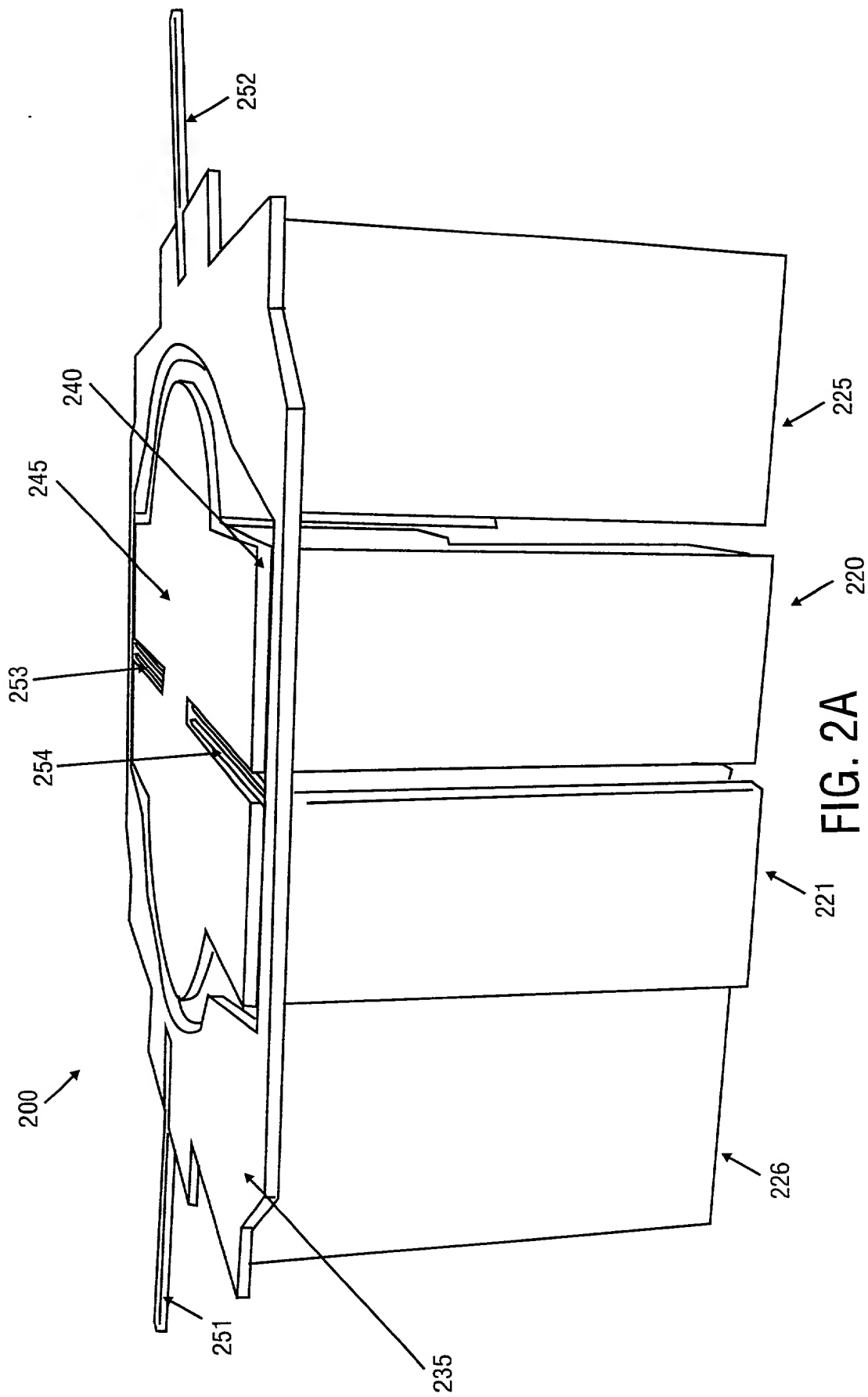


FIG. 1C
(PRIOR ART)





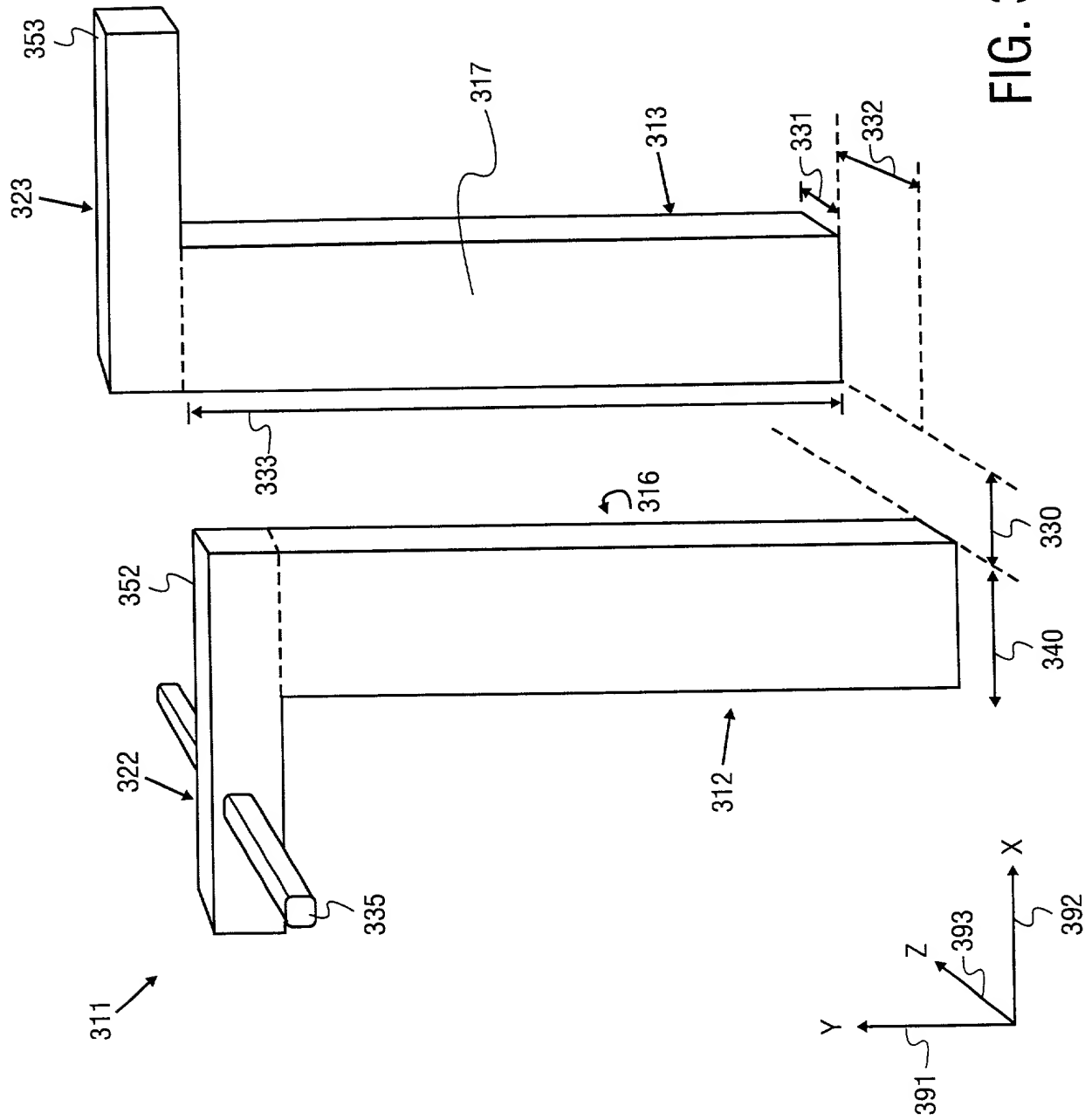


FIG. 3A

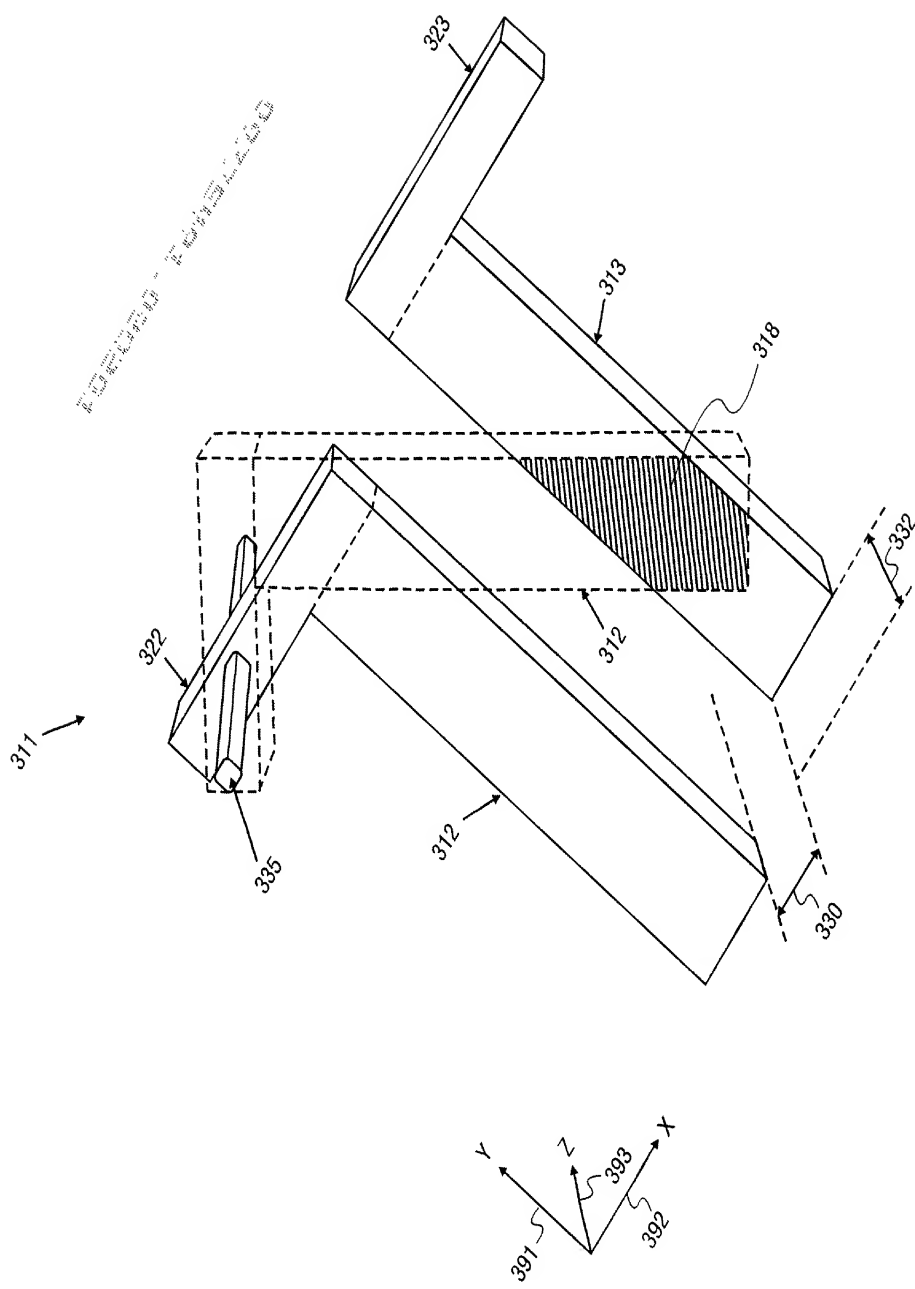


FIG. 3B

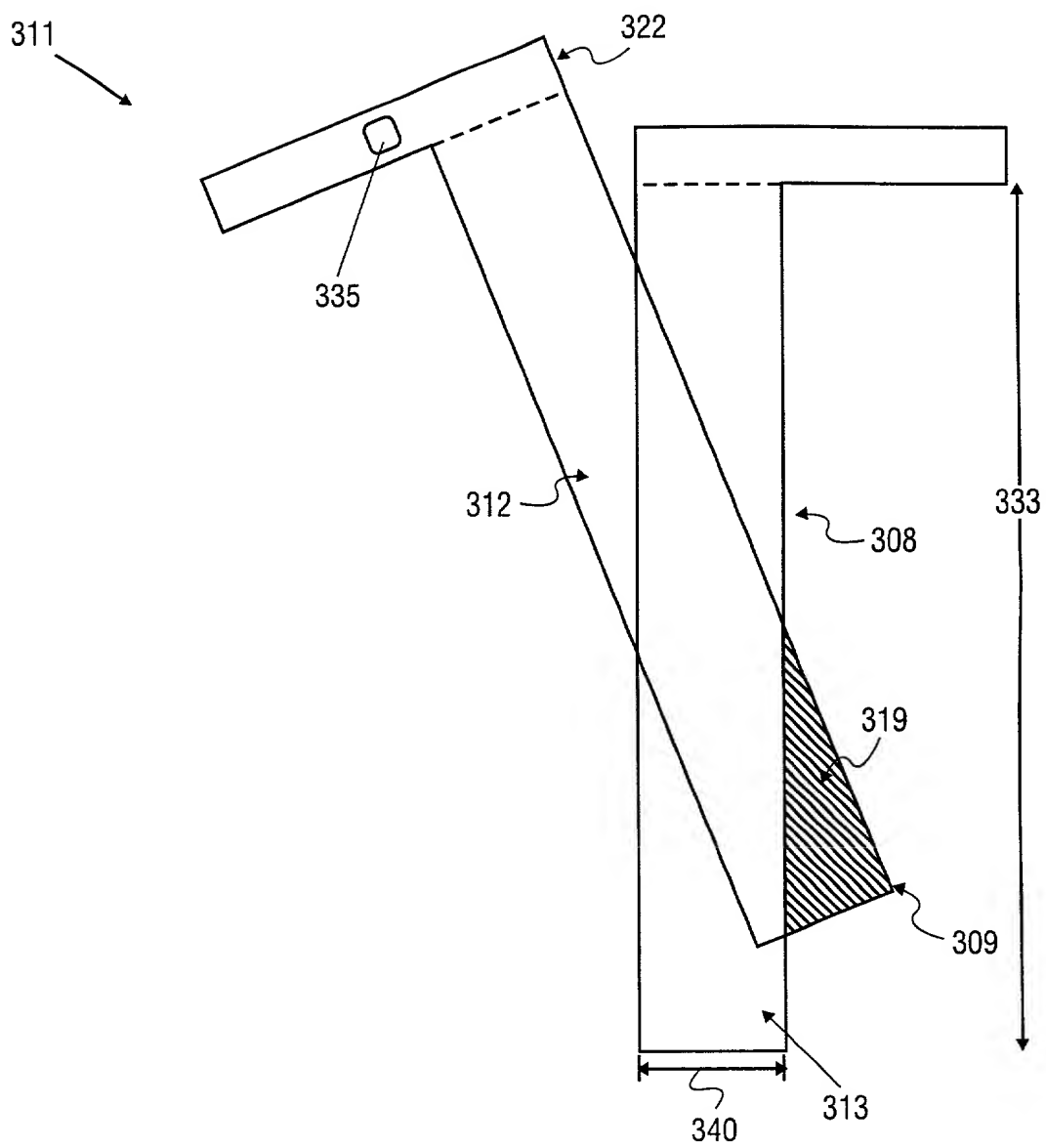


FIG. 3C

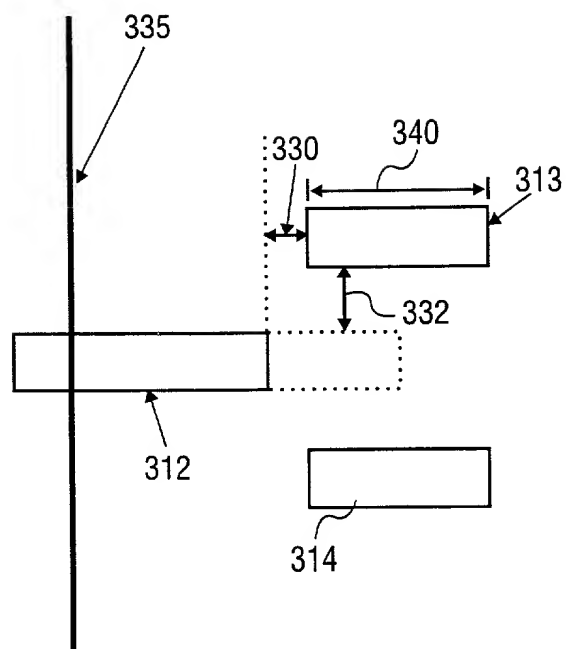


FIG. 3D

FIG. 3E is a cross-sectional view of the device 100, taken along the line 3-3 of FIG. 3A. The device 100 includes a substrate 312, a gate dielectric layer 313, and a gate electrode 314. The gate electrode 314 is disposed on the gate dielectric layer 313 and is electrically connected to a gate terminal 315. The gate electrode 314 is disposed over a channel region 316, which is defined by a pair of side walls 317. The side walls 317 are disposed on the substrate 312 and are electrically connected to a source/drain terminal 318. The side walls 317 are disposed on the substrate 312 and are electrically connected to a source/drain terminal 318. The side walls 317 are disposed on the substrate 312 and are electrically connected to a source/drain terminal 318.

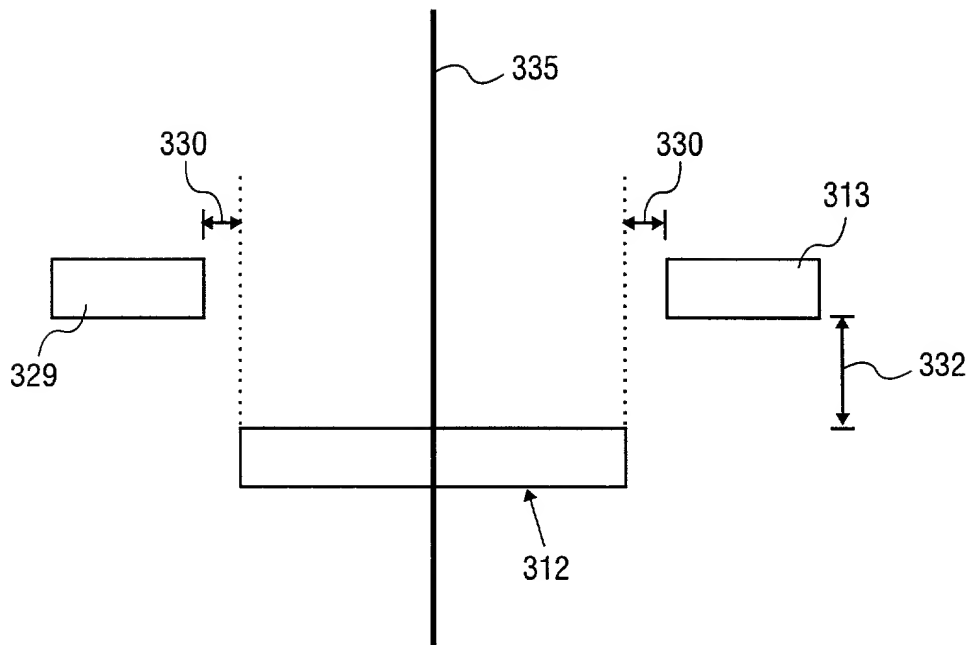
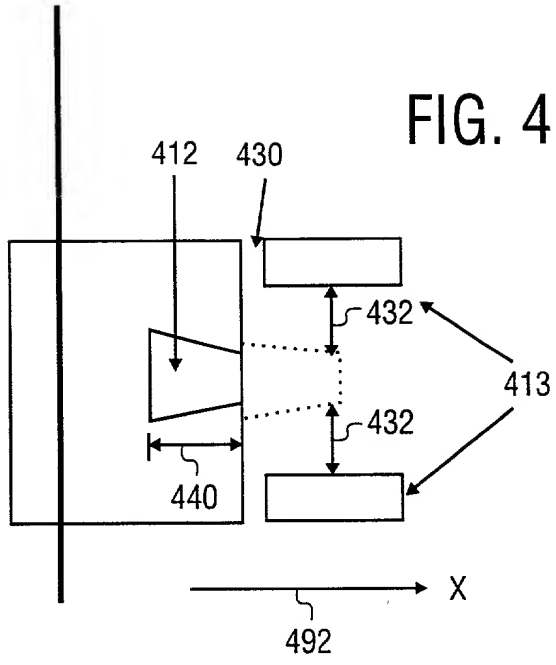


FIG. 3E

FIG. 4 is a schematic diagram of a device 400 in a cross-sectional view. The device 400 includes a substrate 410, a gate stack 412, a gate electrode 413, a channel layer 414, a source/drain region 415, and a contact layer 416. The gate stack 412 is formed on the substrate 410 and includes a gate oxide layer 412a and a gate electrode layer 412b. The gate electrode 413 is formed on the gate stack 412 and is electrically connected to the channel layer 414. The channel layer 414 is formed on the gate electrode 413 and is electrically connected to the source/drain region 415. The contact layer 416 is formed on the source/drain region 415 and is electrically connected to the channel layer 414. The device 400 is shown in a cross-sectional view along a line X-X'.



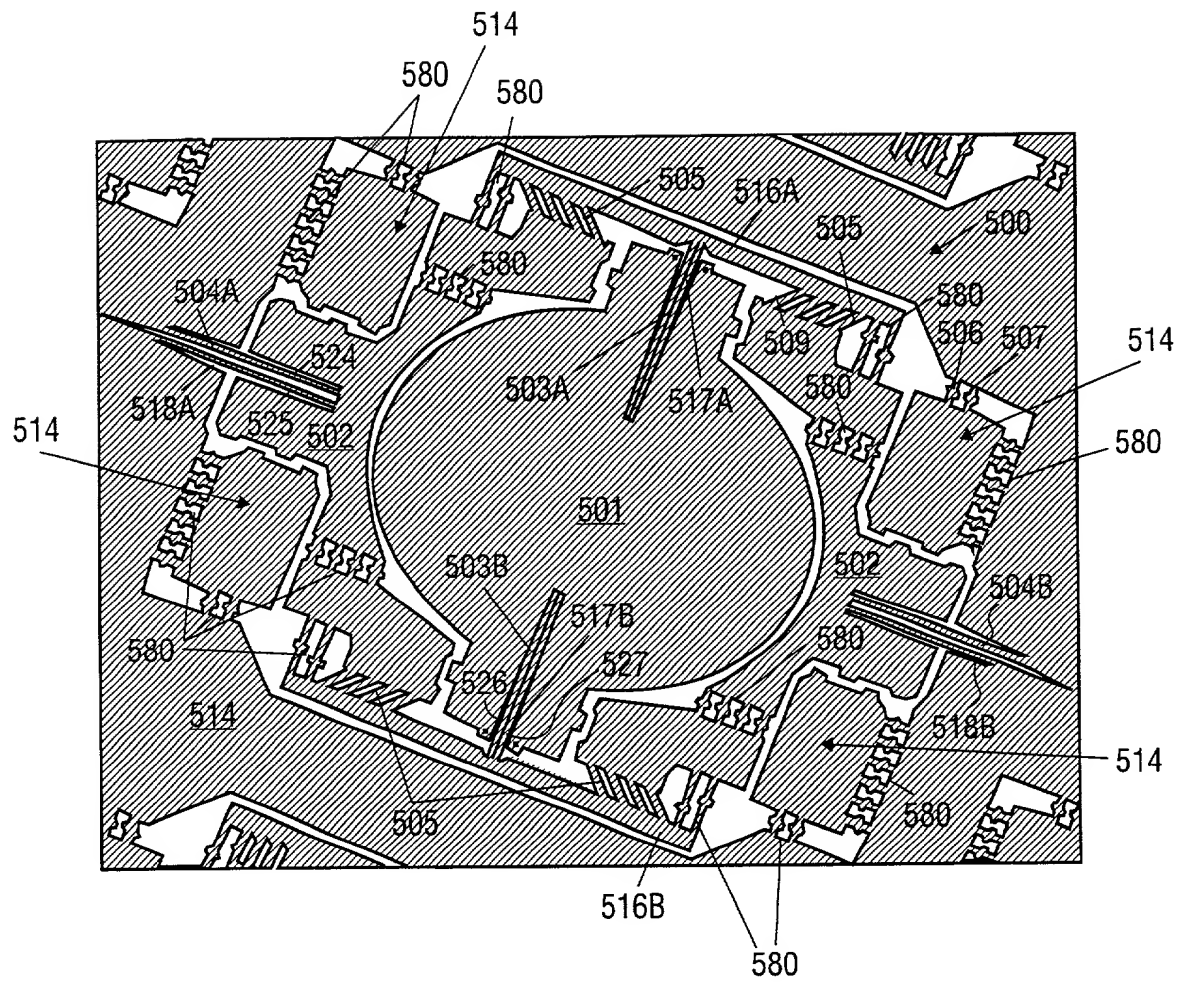


FIG. 5A

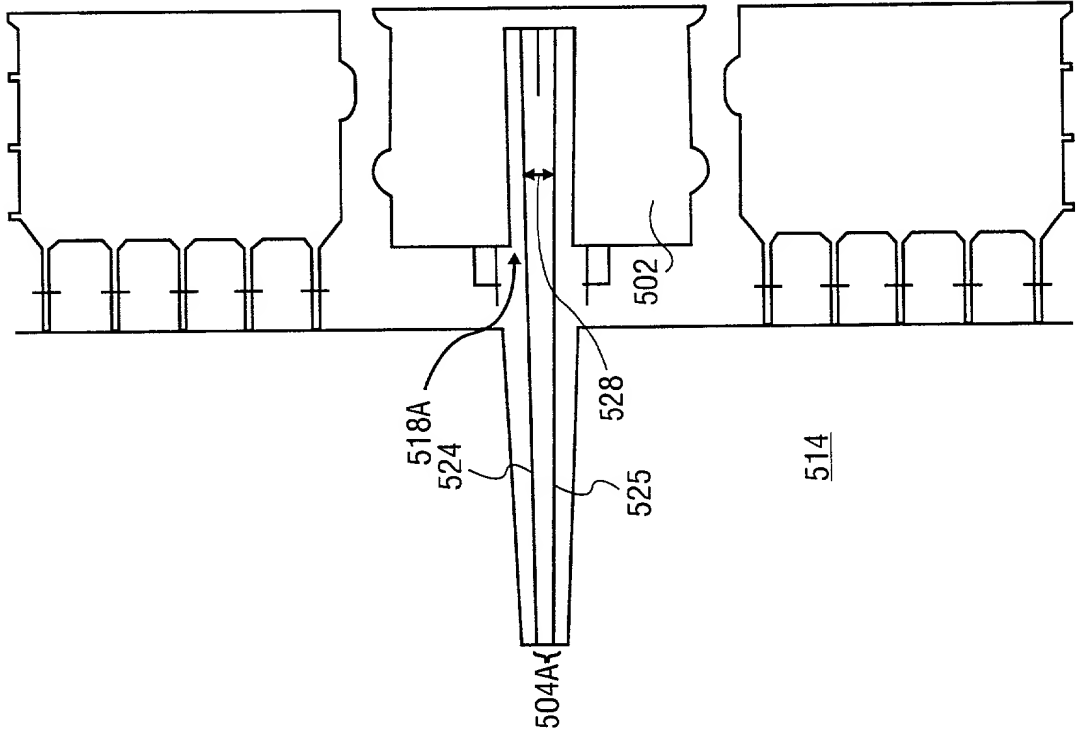


FIG. 5B

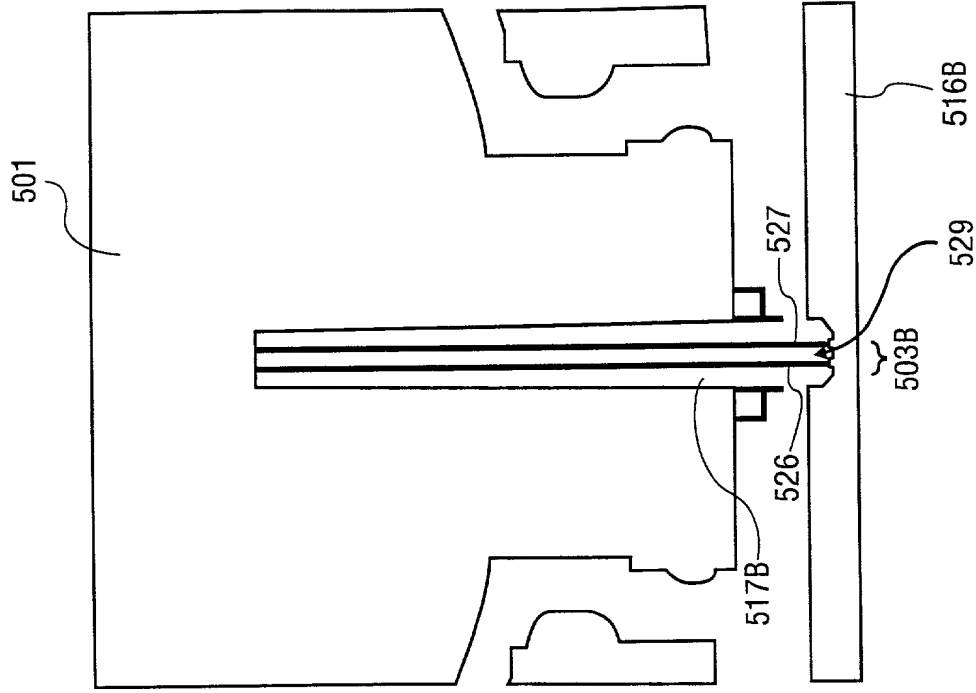


FIG. 5C

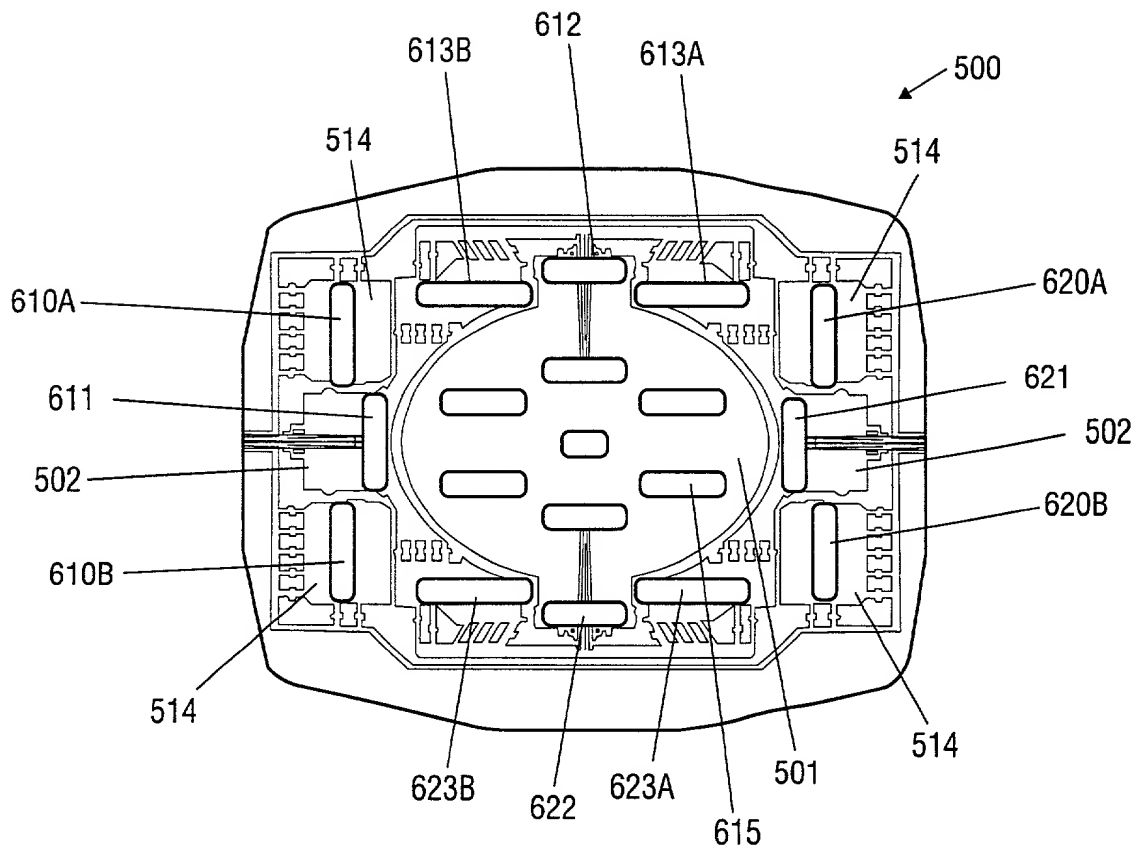


FIG. 6

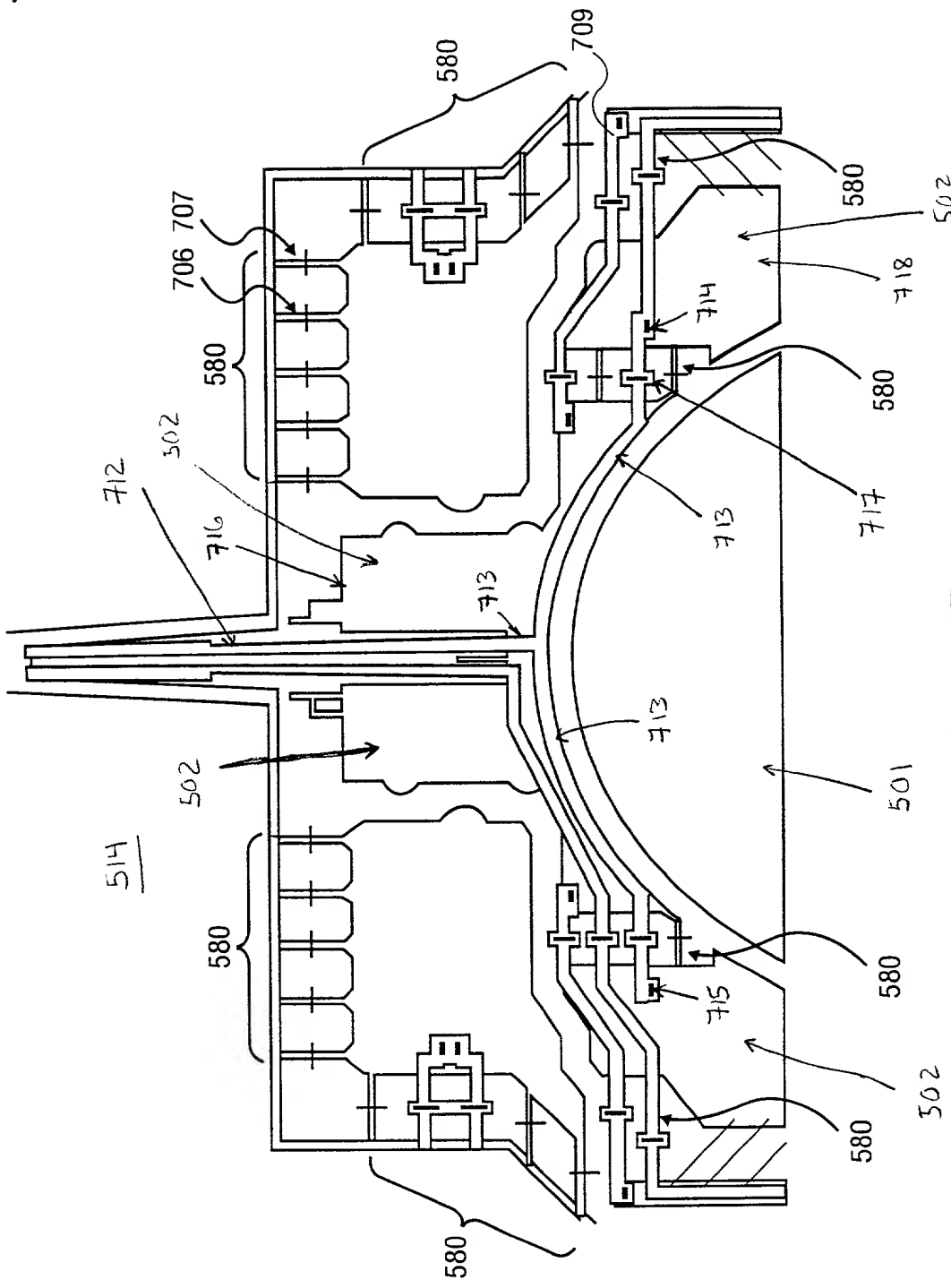


FIG. 7B

FIG. 8 is a top view of a device 500, which is a cross-sectional view of a device 500, showing a central circular region 801, surrounded by a ring of eight rectangular regions 9A-9K, which are arranged in a circular pattern around the central region 801. The device 500 is shown in a cross-sectional view, with the central region 801 being a circular region, and the surrounding regions 9A-9K being rectangular regions arranged in a circular pattern around the central region 801. The device 500 is shown in a cross-sectional view, with the central region 801 being a circular region, and the surrounding regions 9A-9K being rectangular regions arranged in a circular pattern around the central region 801.

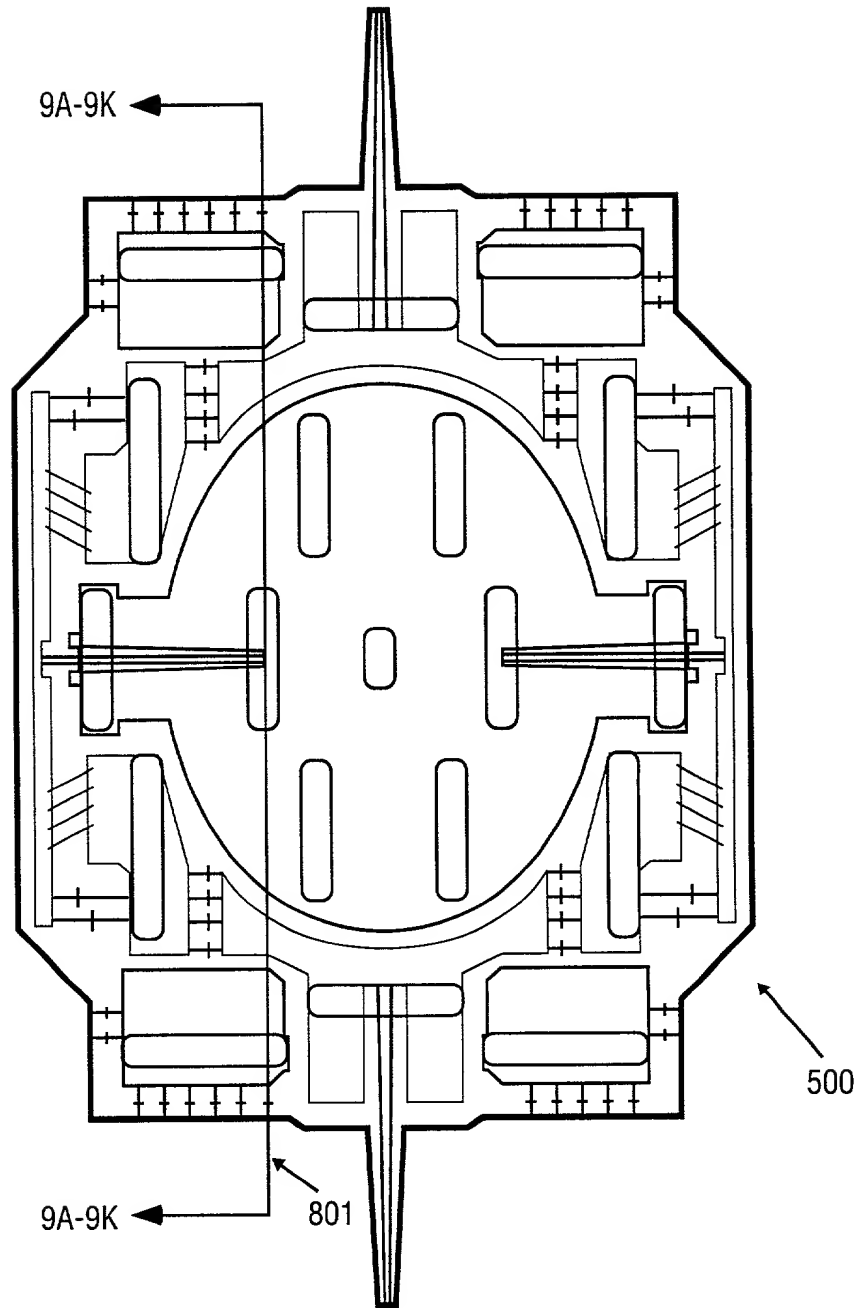


FIG. 8

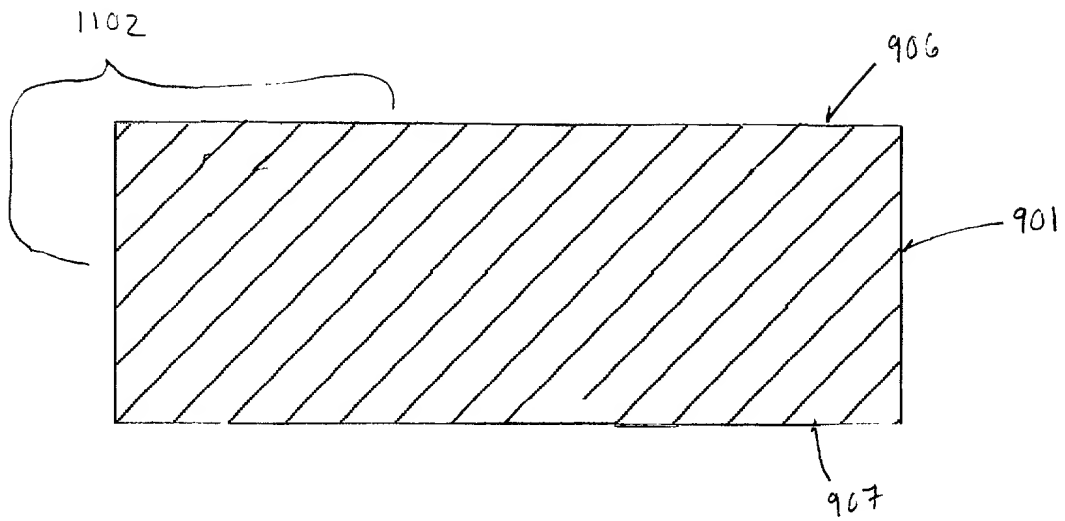


FIG. 9 A

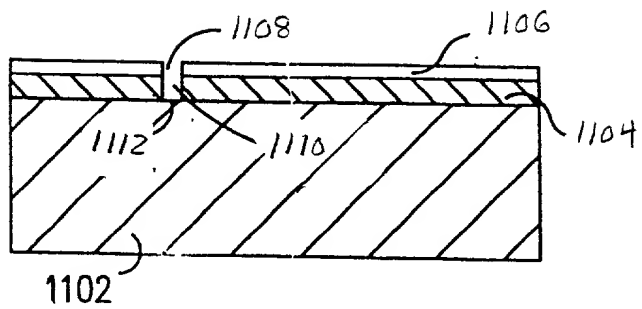


FIG. 9B

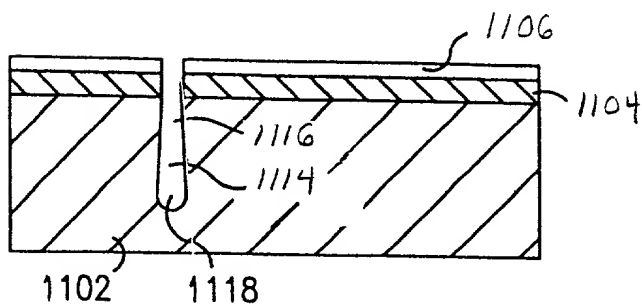


FIG. 9C

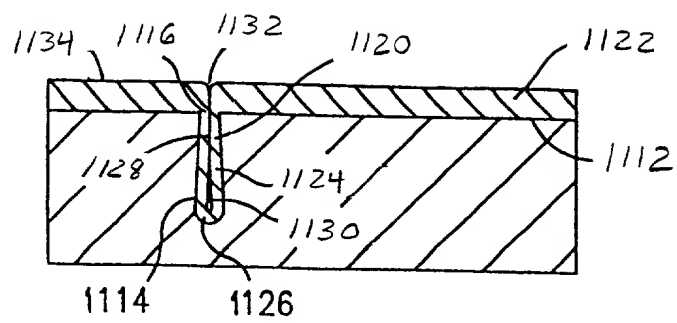


FIG. 9D

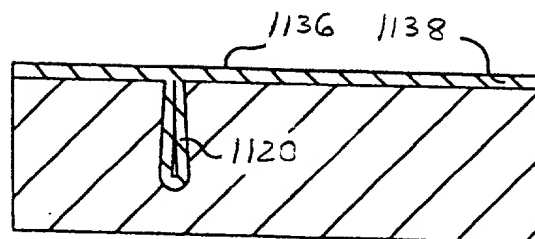
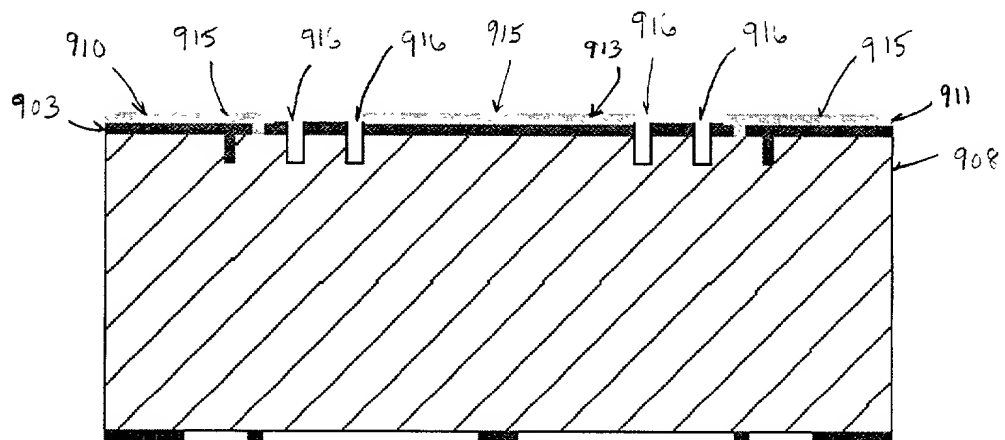
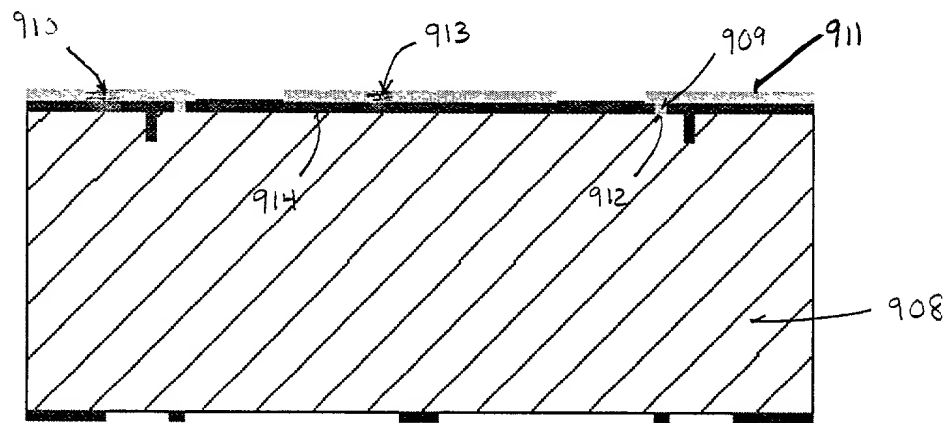
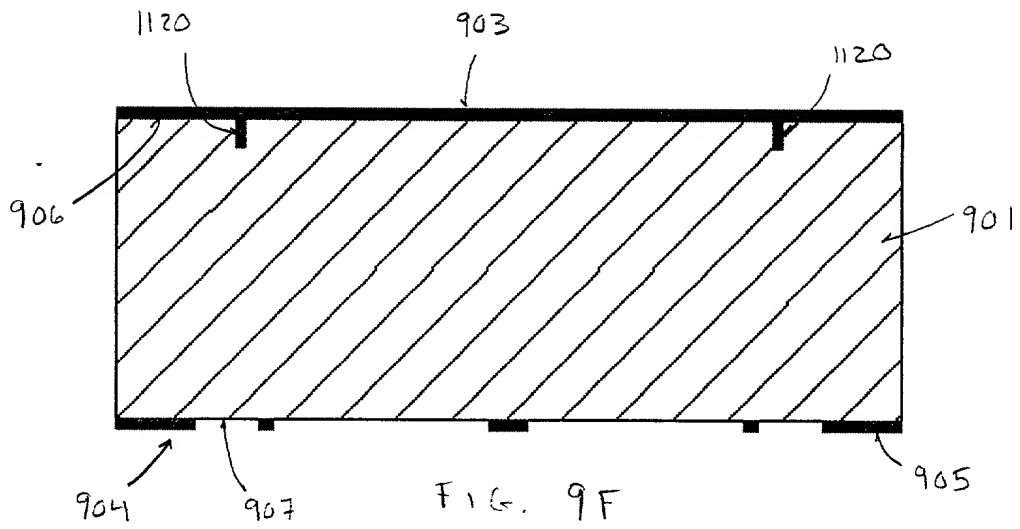
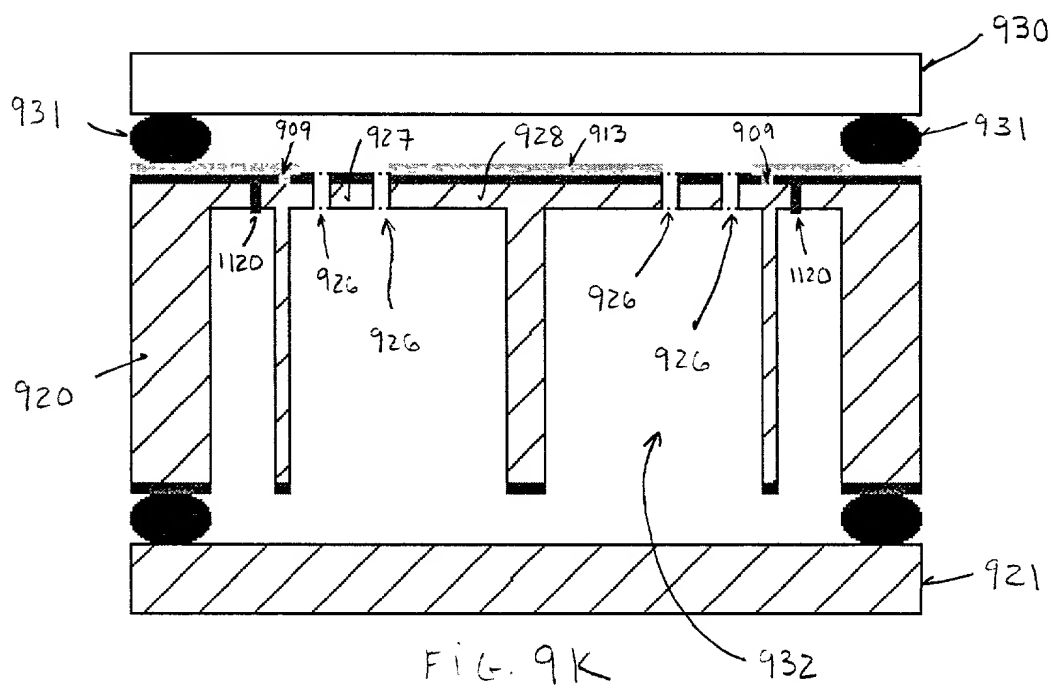
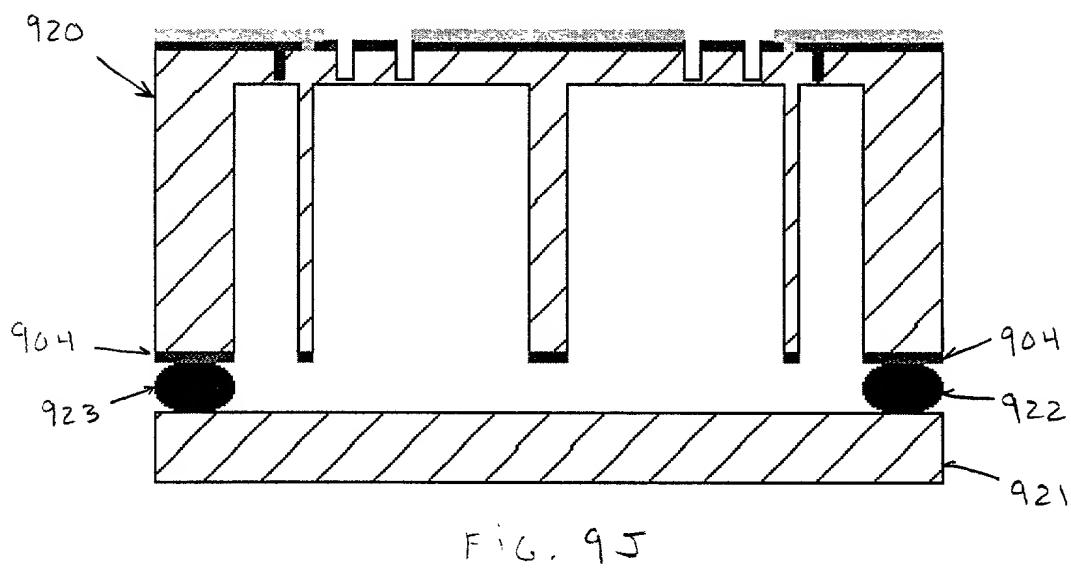
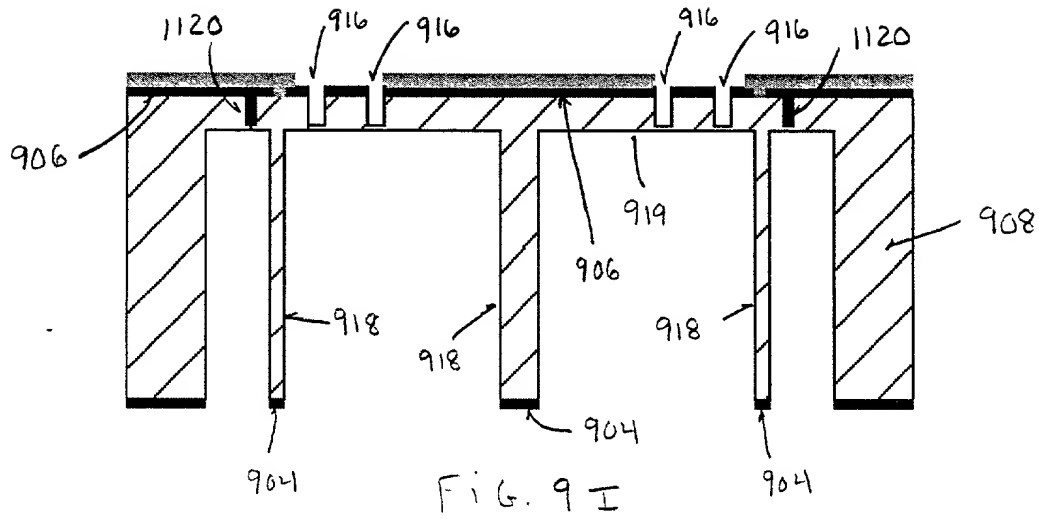
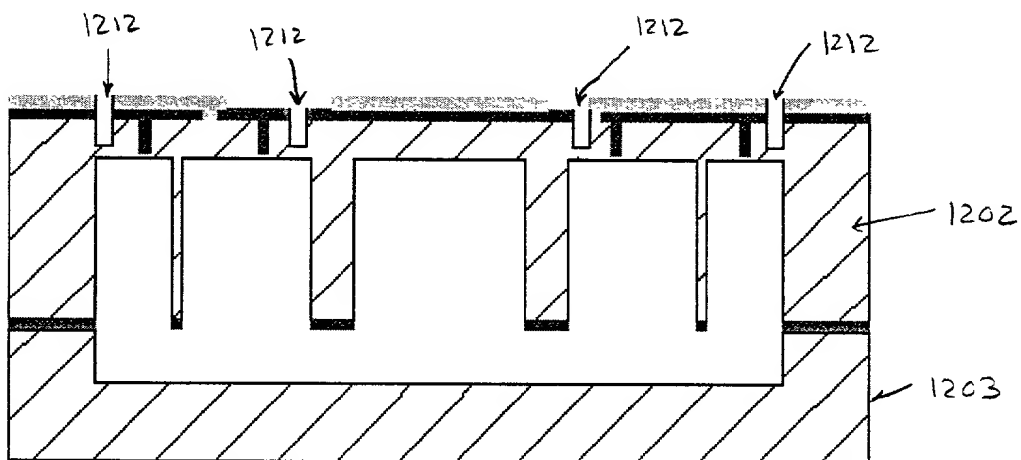
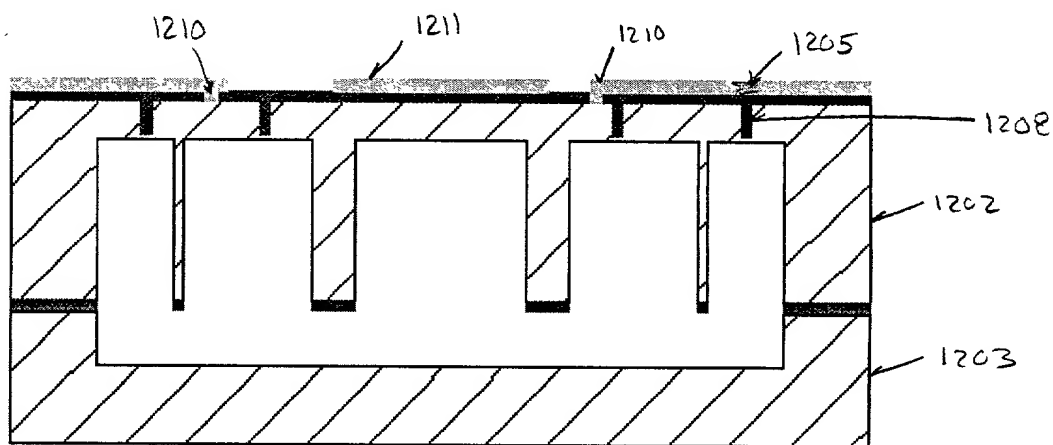
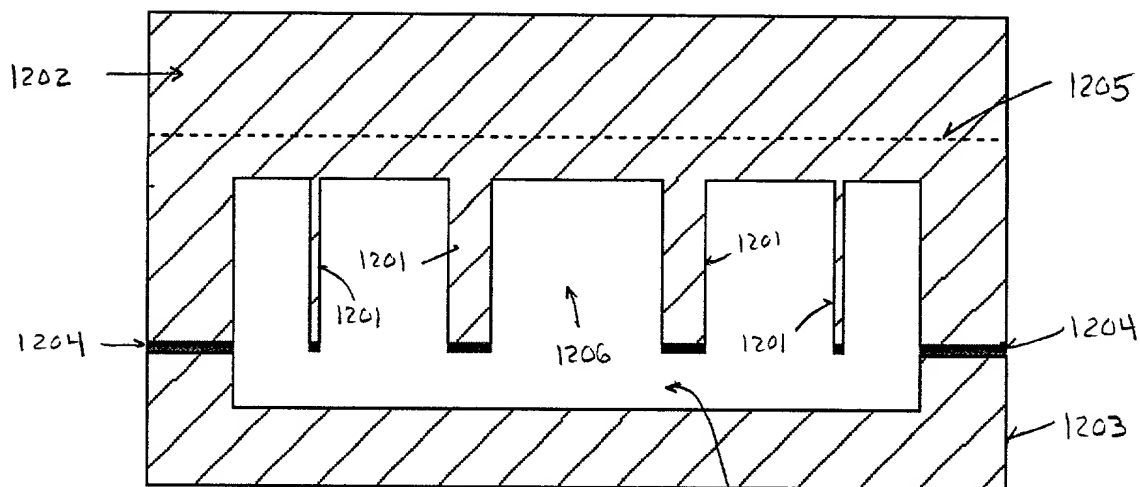


FIG. 9E







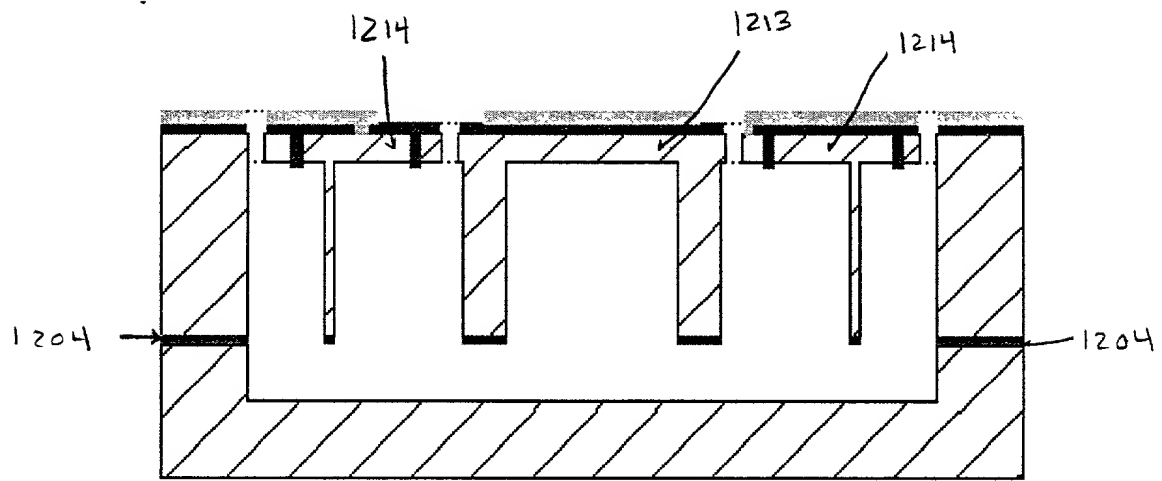


FIG. 10D

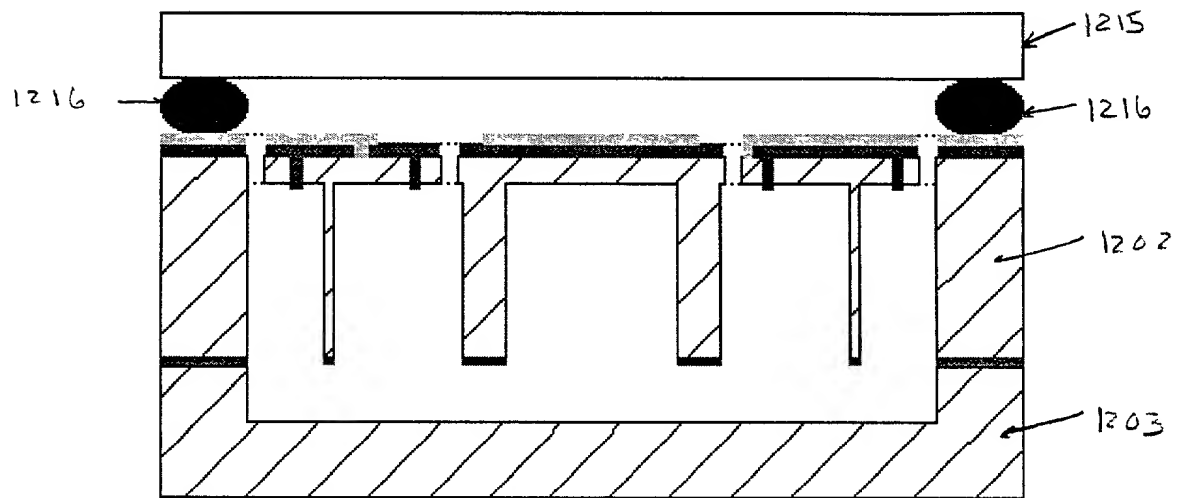


FIG. 10E

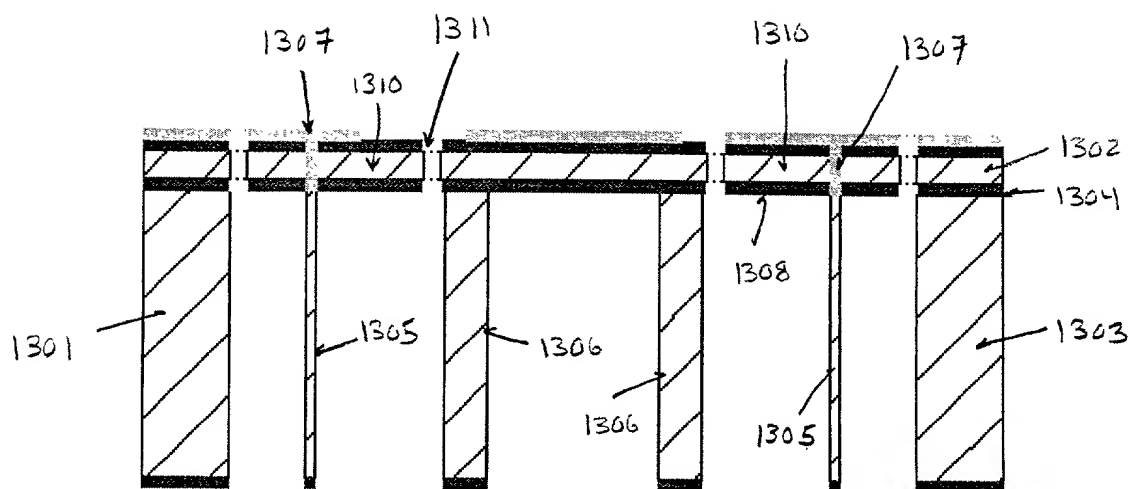
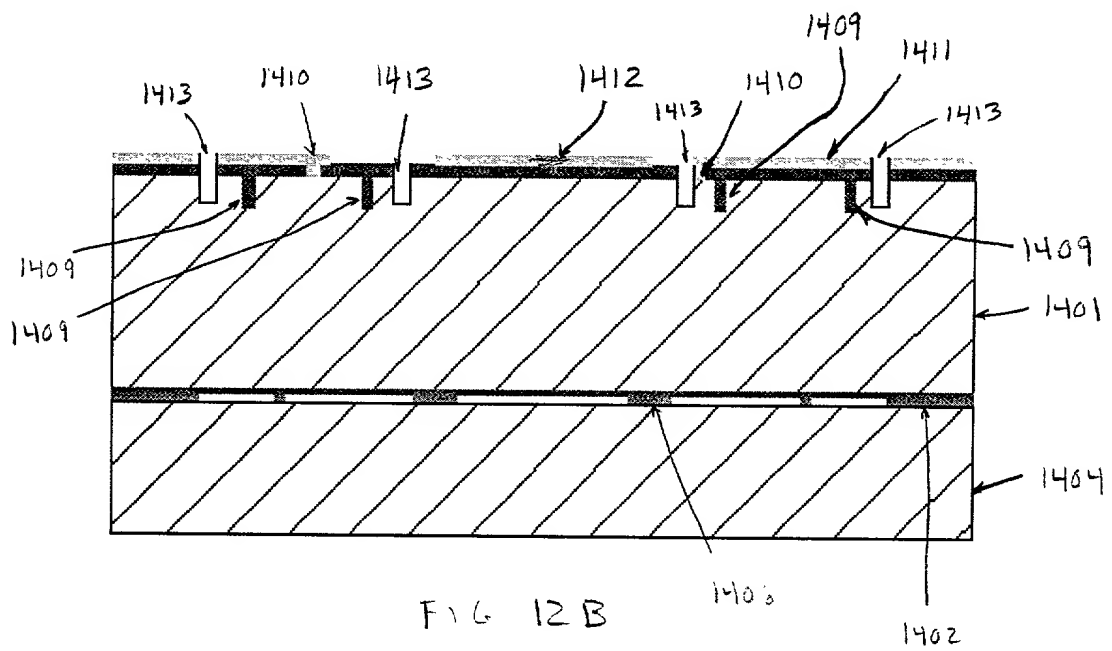
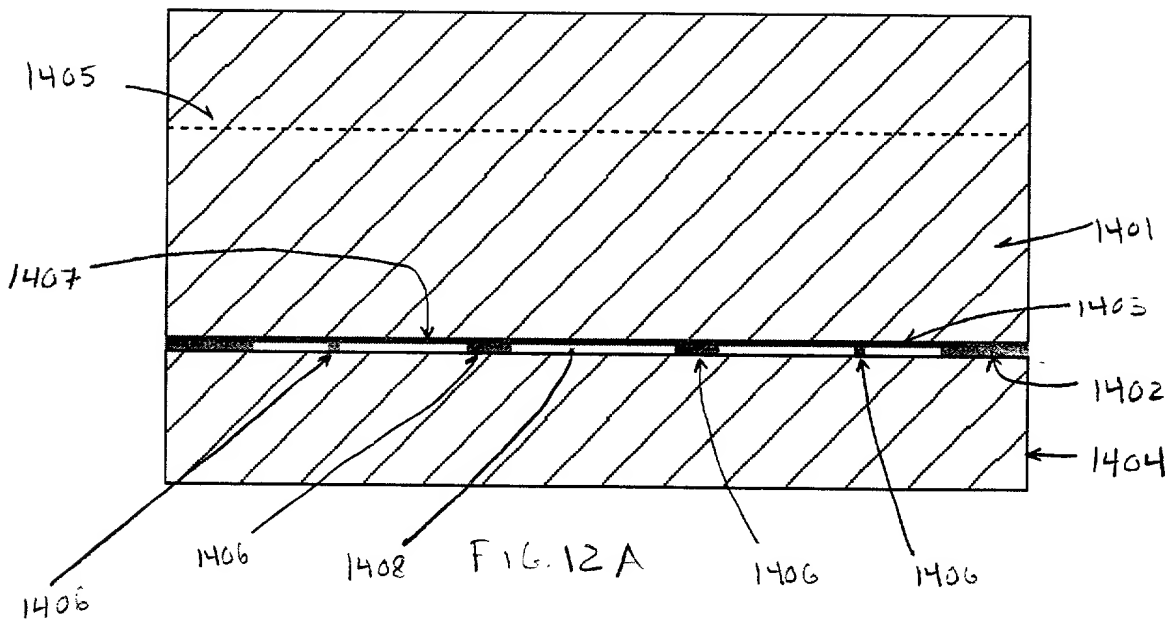


FIG. 11



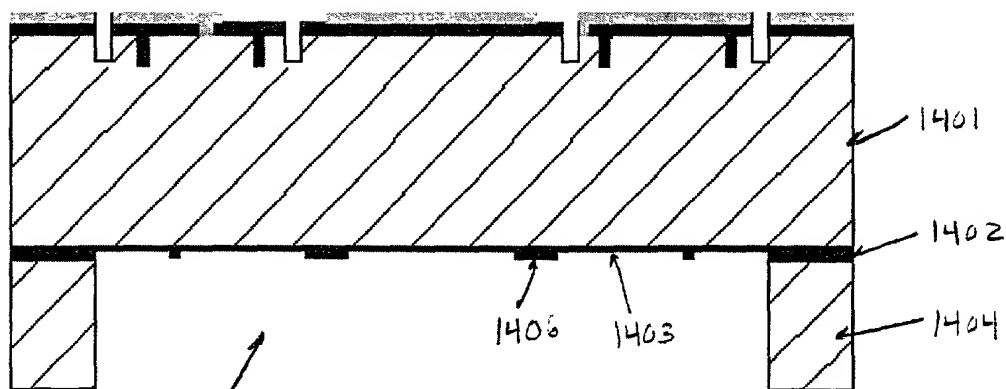


FIG. 12C

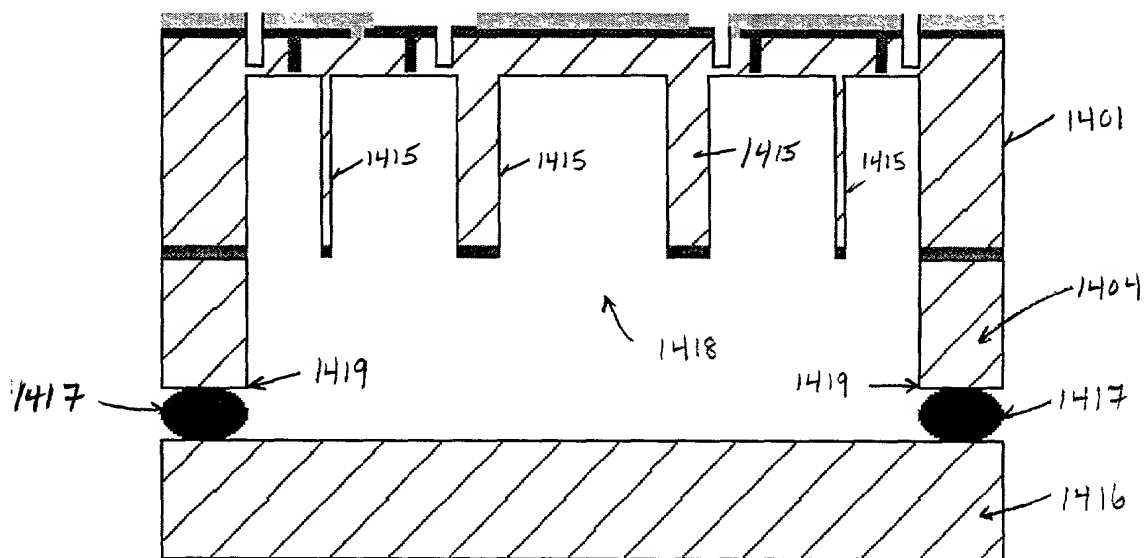


FIG. 12D

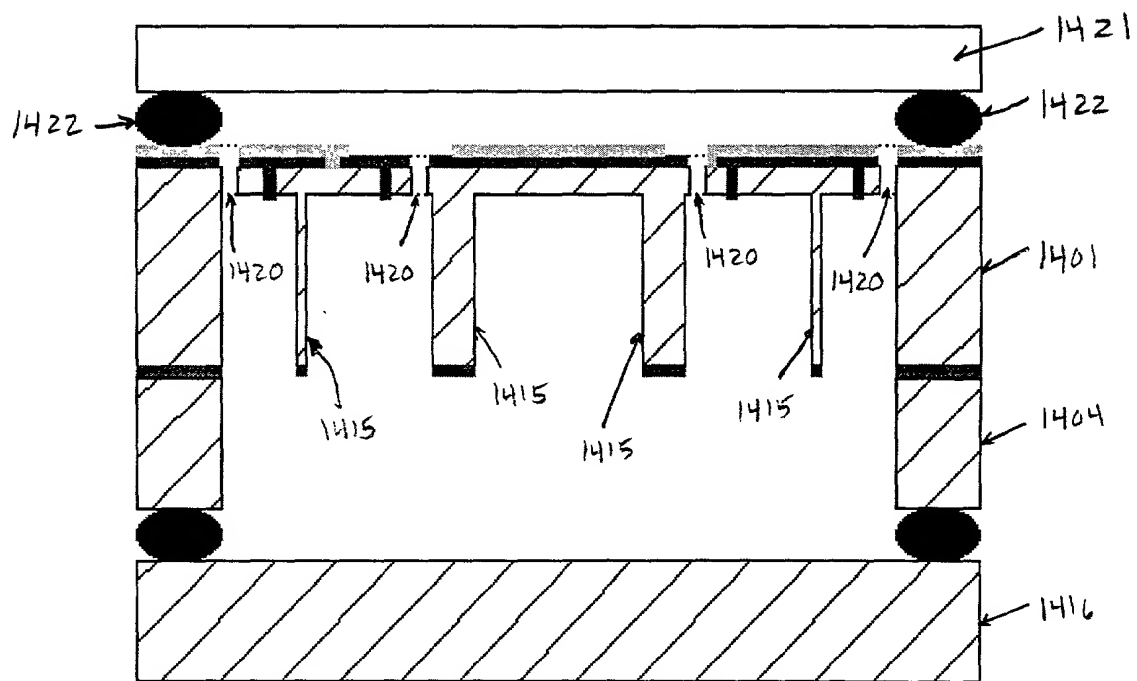


FIG 12E

FIG. 13A

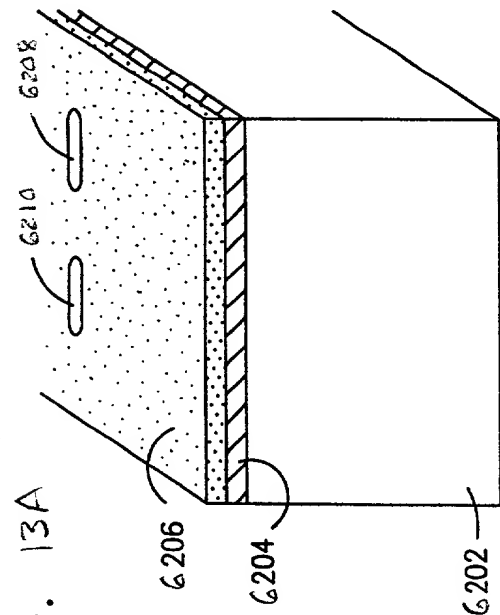


FIG. 13C

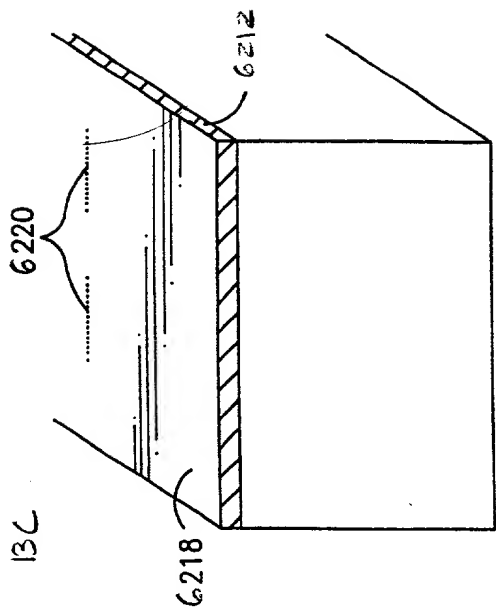


FIG. 13B

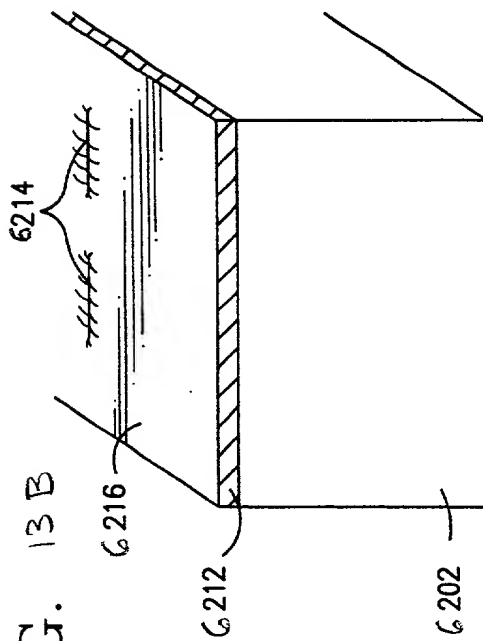
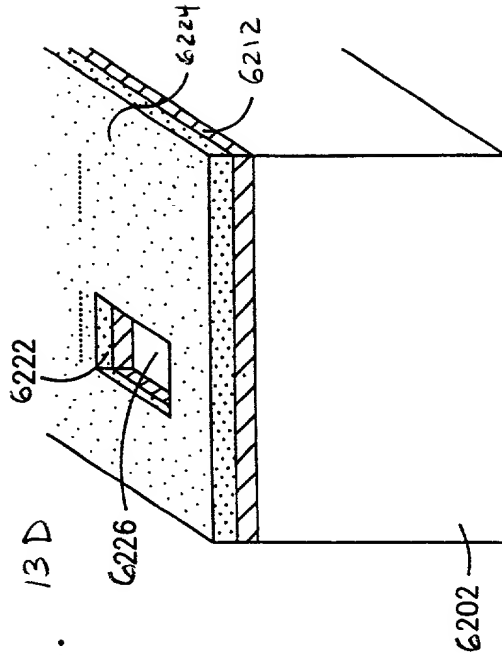


FIG. 13D



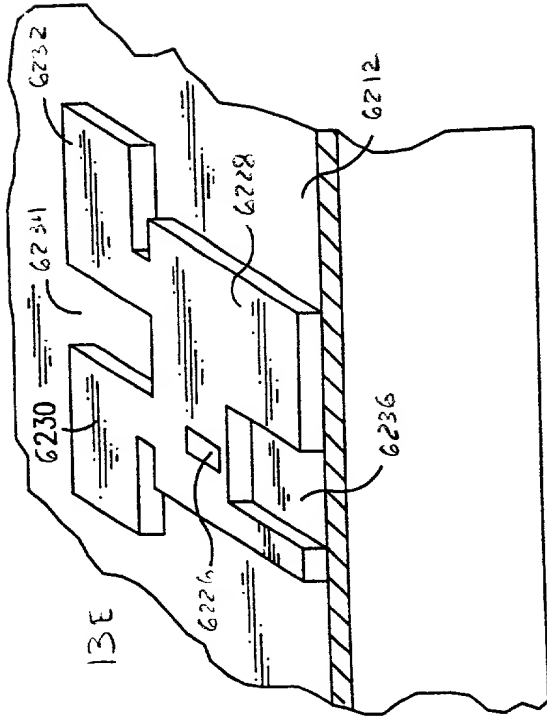


FIG. 13E

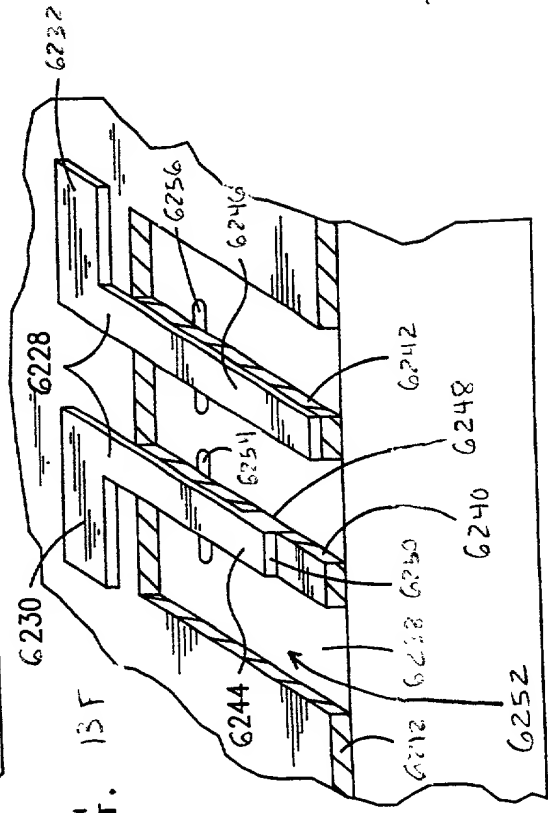


FIG. 13F

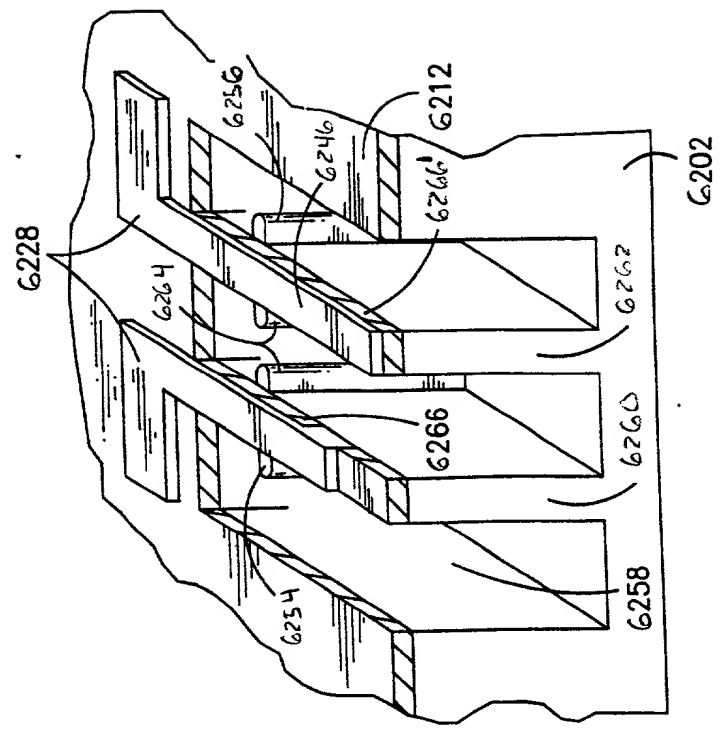


FIG. 13G

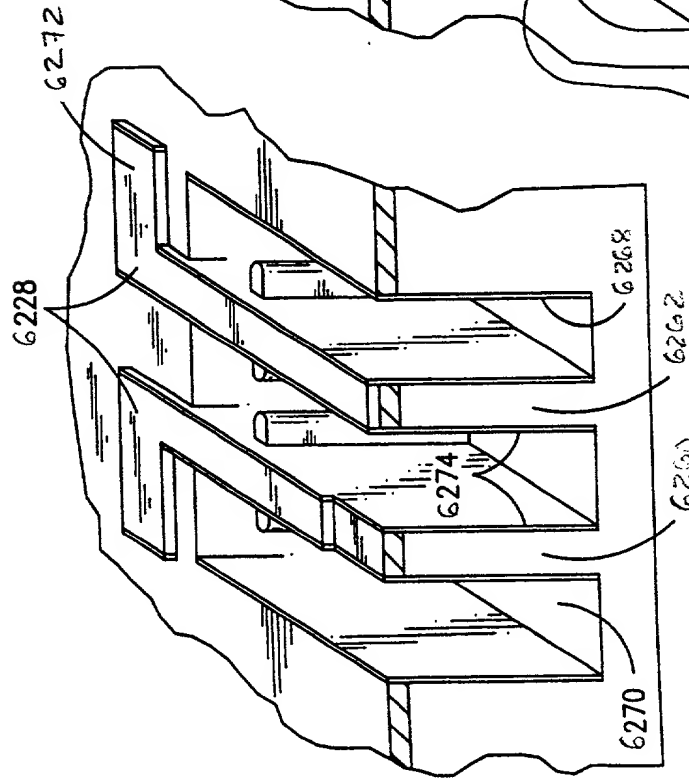


FIG. 13H

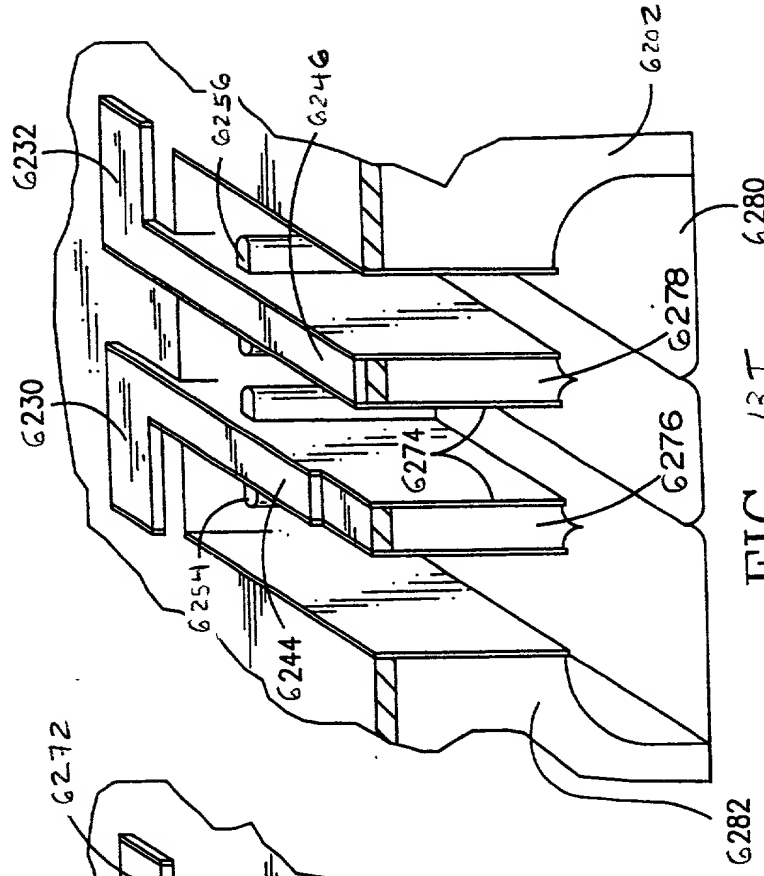


FIG. 13I